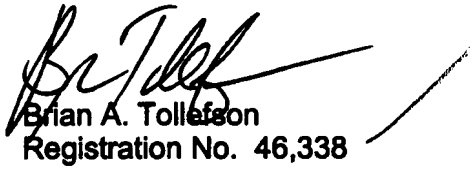
REMARKS

Claims 3-5 have been amended. Page 13 of the specification has also amended. The amendment to Figure 3 has been made to correct the typographical error. No new matter has been added. A Request for Approval of Drawing Changes is attached hereto.

Should there be any questions, the Examiner is invited to contact the undersigned at the below listed number.

Please charge any fee deficiency which may be due with respect to this paper, or credit any overpayment, to our Deposit Account No. 01-2300 referencing docket number 107346-00017.

Respectfully submitted,



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Enclosures: Request for Approval of Drawing Corrections
Marked-Up Copy

MARKED UP COPY OF AMENDED SPECIFICATION

Please amend the paragraph beginning at line 10 of page 13 as follows:

(S7) If N [<] ≥ K, then the process goes to step S8, and if N = K, then the process goes to step 9.

MARKED UP COPY OF AMENDED CLAIMS

3. (Twice Amended) The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step up said second bias current in response to judgment that a value obtained by said successively summing is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease operation [of said bias adjustment circuit] thereof in response to judgment that said value obtained by said successively summing is smaller than said reference value

4. (Twice Amended) The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively summing is smaller than said reference value by said comparator circuit, and

wherein said control circuit is configured to cease operation [of said bias adjustment circuit] thereof in response to judgment that said value obtained by said successively summing is larger than said reference value.

5. (Twice Amended) The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively summing is smaller than said reference value by said comparator circuit, and step up said second

bias current in response to judgment that said value obtained by said successively summing is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease operation [of said bias adjustment circuit] thereof in a case where an absolute value of a difference between said value obtained by said successively summing and said reference value is smaller than a given value.